

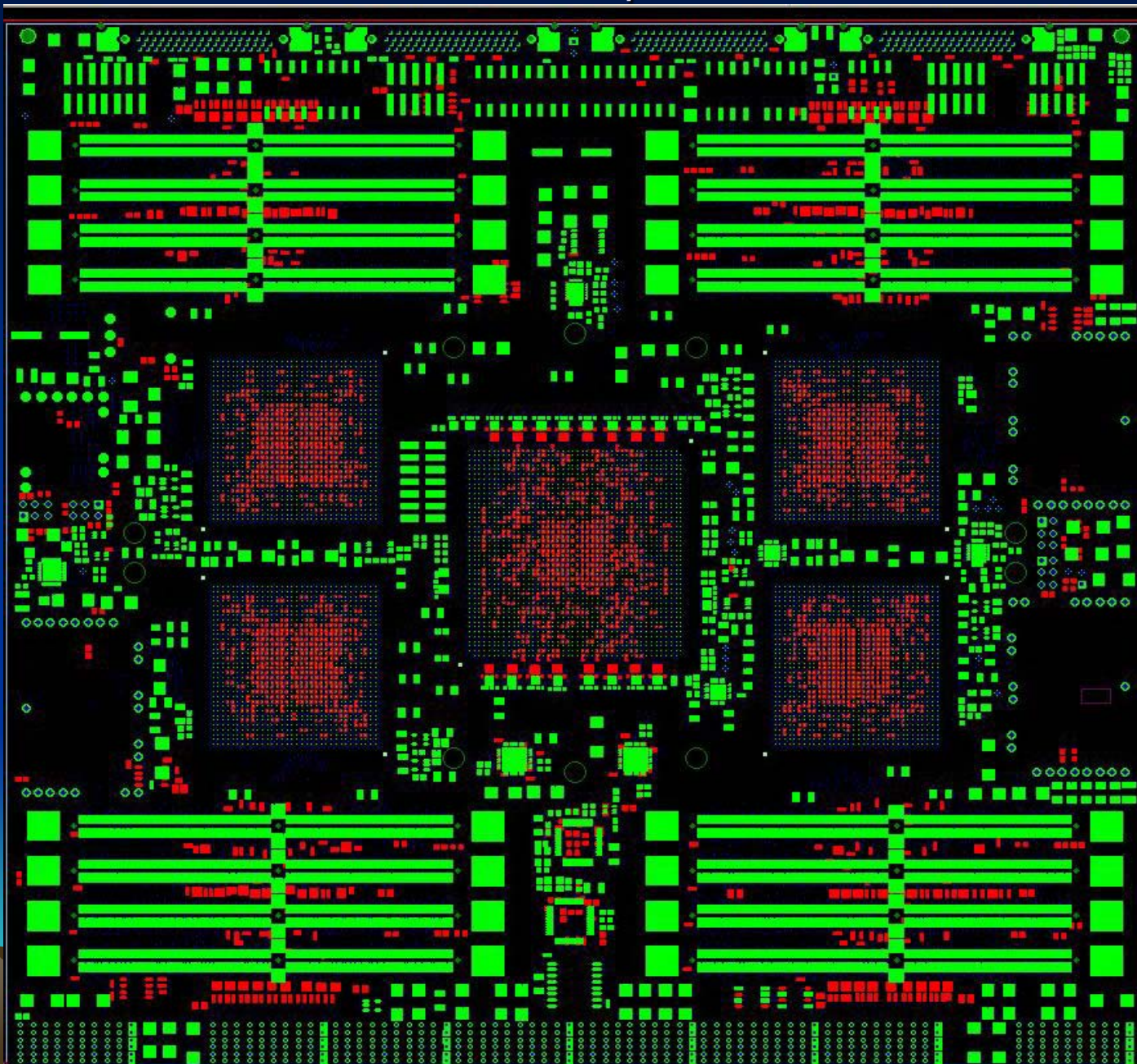
Проблемы внедрения новых технологий для проектирования и производства печатных плат

Технология HDI

Петров А.О. 16.12.2010



Традиционная технология металлизированных сквозных отверстий себя исчерпала



Определение HDI

Definitions / Standards of HDI

IPC-2226 definition of HDI and microvia

High Density Interconnect

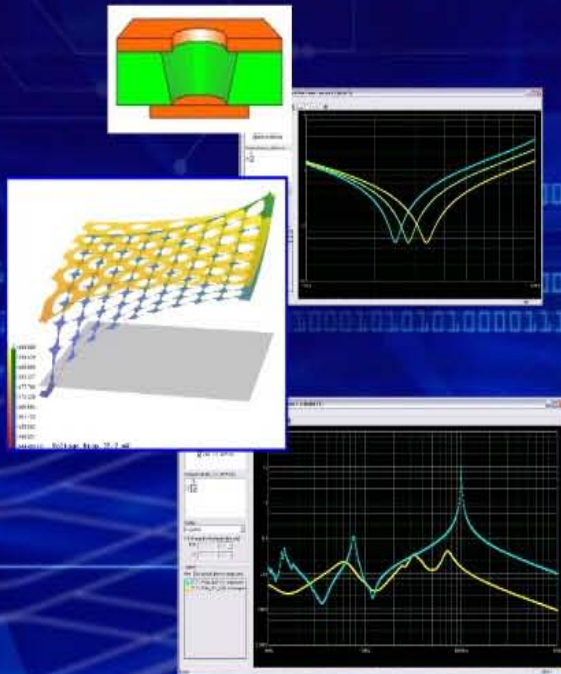
Printed circuit board with a higher wiring density per unit area than conventional printed circuit boards (PCB). They have finer lines and spaces ($\leq 100 \mu\text{m}$), smaller vias ($< 150 \mu\text{m}$) and capture pads ($< 400 \mu\text{m}$), and higher connection pad density ($> 20 \text{ pads/cm}^2$) than employed in conventional PCB technology.

Microvia

A blind hole with a diameter ($\leq 150 \mu\text{m}$) having a pad diameter ($\leq 350 \mu\text{m}$) formed by either laser or mechanically drilling.

Power Integrity Effects of High Density Interconnect (HDI)

Patrick Carrier
Technical Marketing Engineer
Patrick_Carrier@mentor.com



© Mentor Graphics Corp. Reuse by written permission only. All rights reserved.

Mentor Graphics®

Power Integrity Effects

of High Density Interconnect (HDI)



Patrick Carrier
Technical Marketing Engineer
Contact

Outline Thumb Notes Search

| Slide Title | Duration |
|-----------------------------|----------|
| ▶ Power Integrity Effect... | 00:16 |
| Agenda Power Integri... | 00:34 |
| Intro to HDI | 00:36 |
| Developing HDI Boards | 01:01 |
| Dielectrics used in HDI | 00:35 |
| Via formation | 00:35 |
| Via formation methods | 00:51 |
| Via metallization | 00:25 |
| Alternative Stackups ... | 00:34 |
| Intro to PI | 01:08 |
| PDN Impedance | 01:24 |
| Capacitors | 01:37 |
| Capacitor Parasitics | 00:47 |
| Low PDN impedance | 00:41 |
| PI and HDI | 01:13 |
| Agenda Power Integri... | 00:09 |
| Fine-pitch BGAs | 00:44 |
| Plane Perforation | 00:56 |
| DC Drop | 00:28 |
| High Current Densities | 00:21 |

31 Minutes 6 Seconds Remaining



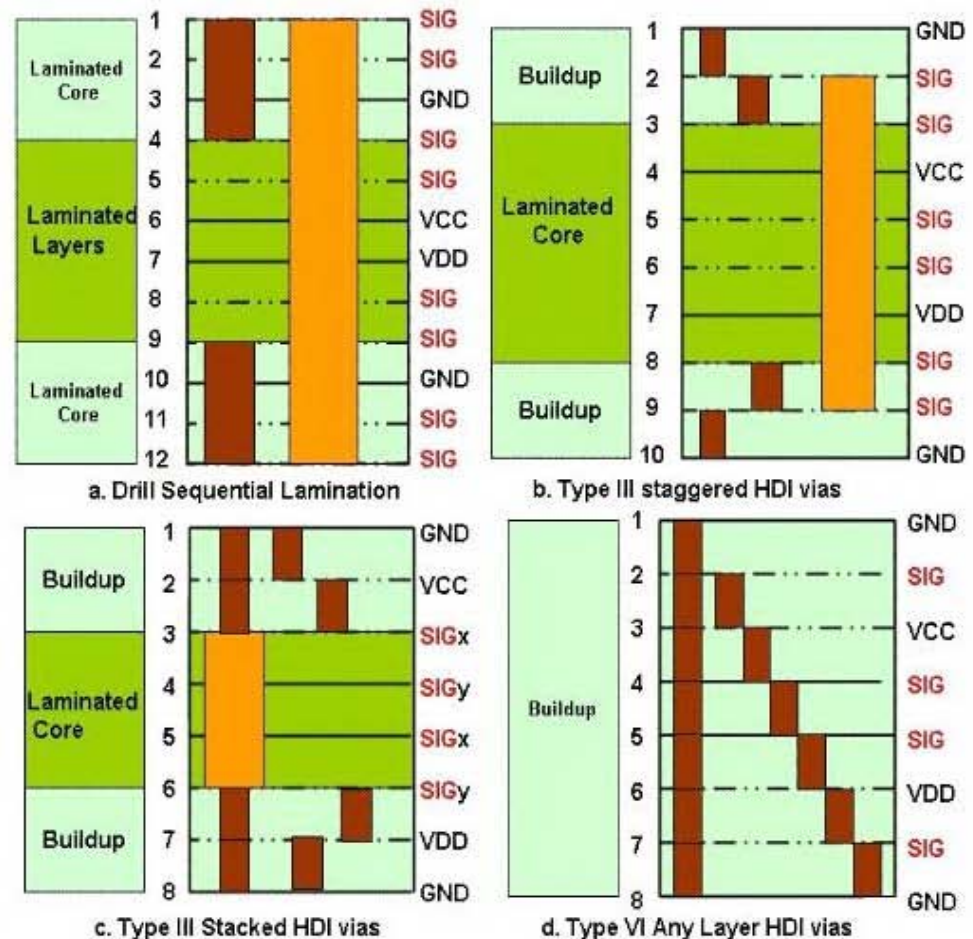
Slide 1 / 47 | Stopped

00:00 / 00:16



Alternative Stackups using HDI

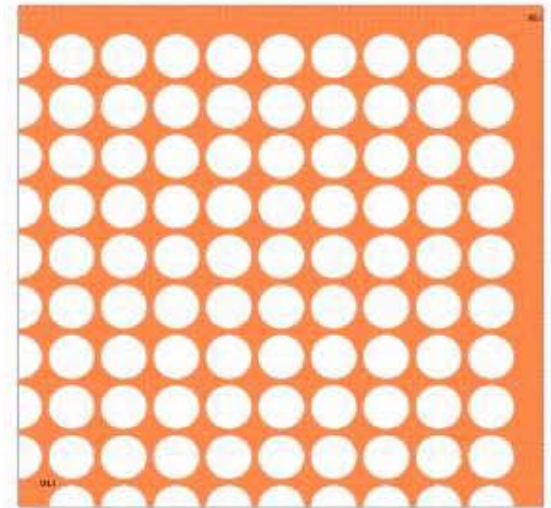
- a. Sequential lamination & drill, 12L
- b. Type III staggered-vias, 10L
- c. Type III Stacked-vias, 8L
- d. Type VI Any-layer vias, 8L



Plane Perforation

- **Example: 1-mm pitch BGA**

- **Field of antipads**
- **Narrow web of copper for**
 - **AC power delivery**
 - **DC power delivery**
- **High in inductance and resistance**

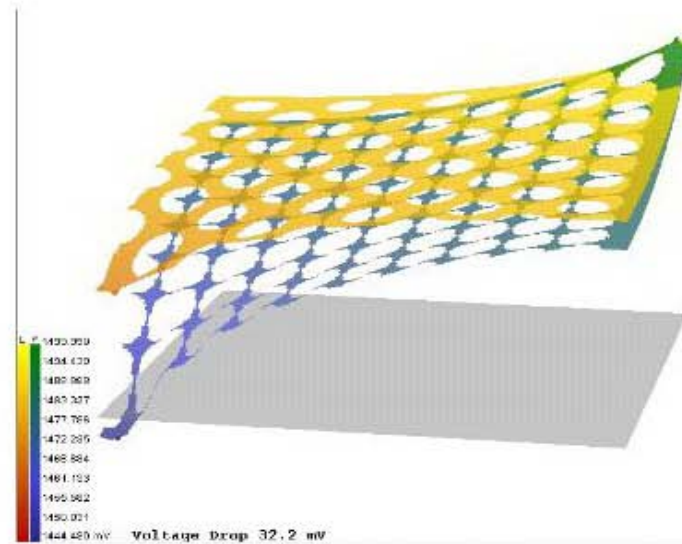
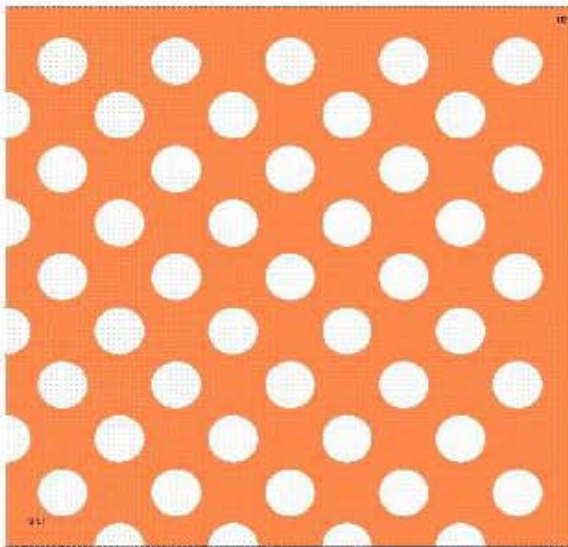


- **Affects power pins**

- **Separated from rest of plane by signal pins**
- **Separated from rest of plane by ground pins**
- **Separated from rest of plane by other power pins**

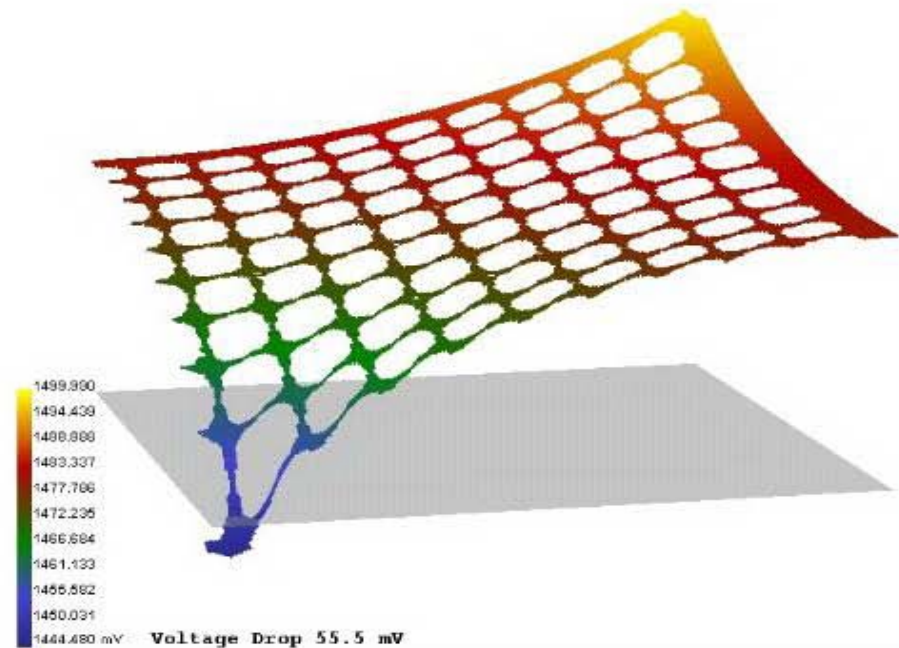
Use of blind vias

- Pins connected only to necessary layers
- Eliminates extra antipads on plane layers
- Can divide number of antipads in half
 - For example, if blind vias were used for ground



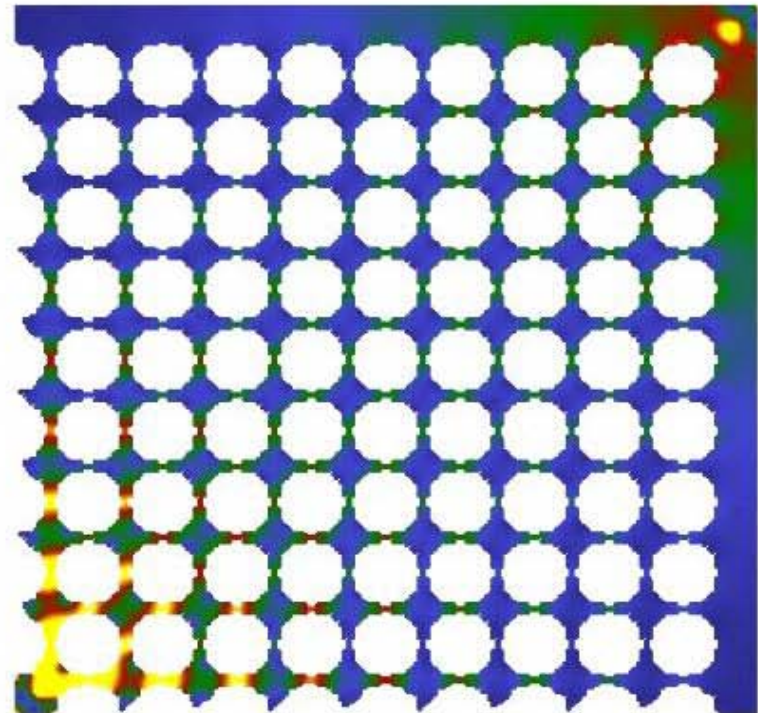
DC Drop

- PDN should have a low impedance at AC and DC
- At DC, series resistance results in DC voltage drop
- Results in:
 - Reduced voltage margins
 - Possible signal integrity problems
 - Core logic malfunction



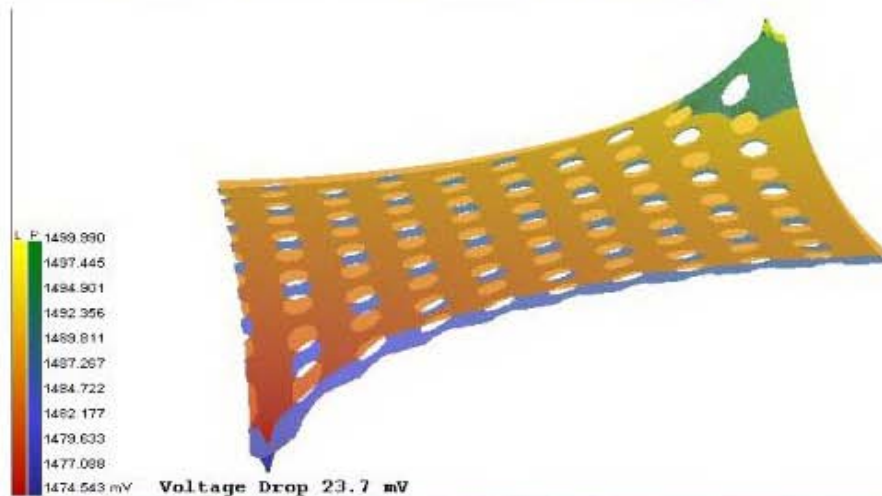
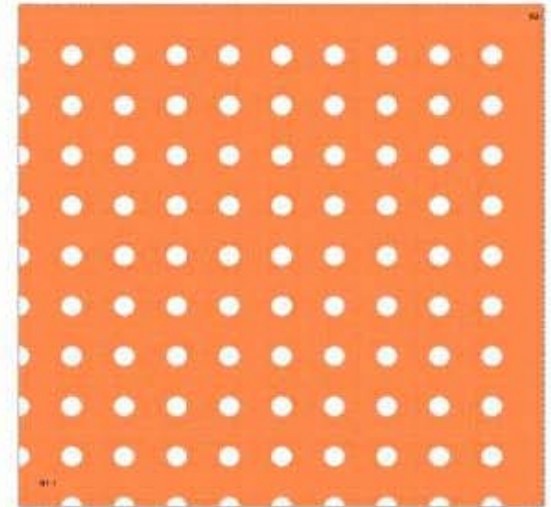
High Current Densities

- Plane perforation also causes high current densities
- Results in
 - DC Drop
 - Board overheating
 - Copper failure
 - Via failure
 - Disconnected power



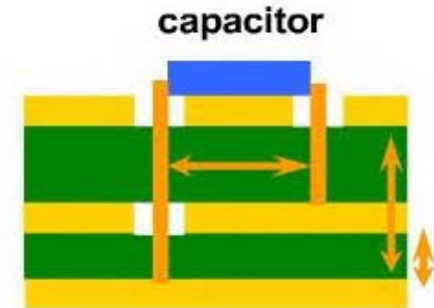
Use of microvias

- Very small antipad size
- More copper for power delivery
- Effects even more noticeable with removal of some antipads



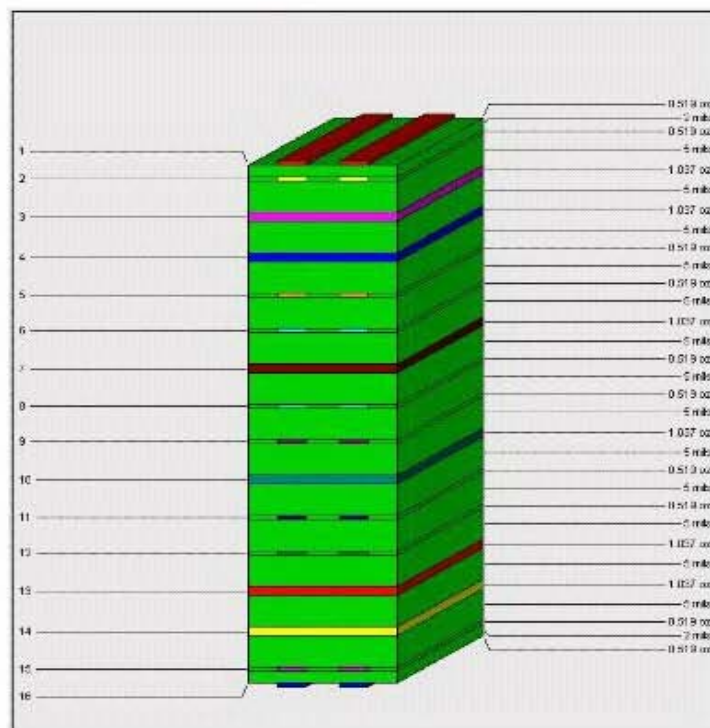
Mounting Inductance

- **Minimized by reducing size of loop area connecting power and ground**
- **Connection from top/bottom of board through vias**
- **Mounting inductance dominated by**
 - **Via length**
 - **Via separation**
- **Power and ground planes as close to the top as possible facilitates:**
 - **Reduction in via length**
 - **Possibility for antipad removal**



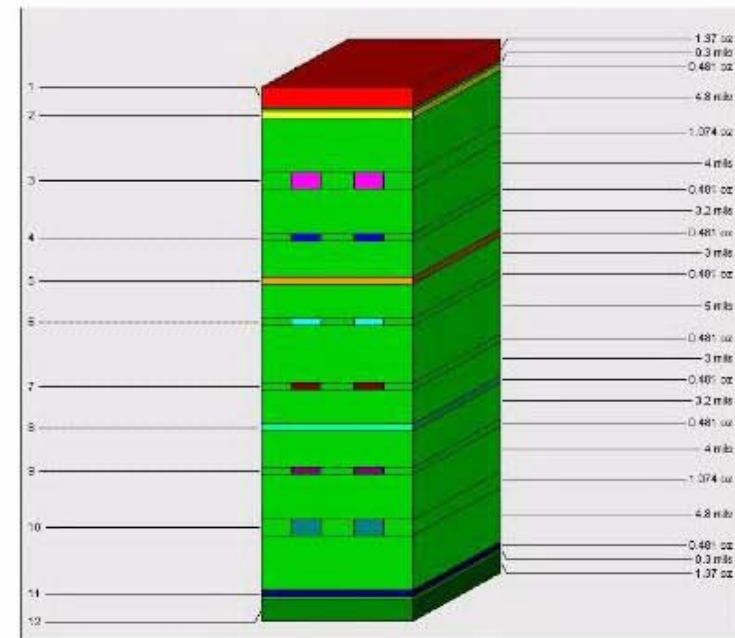
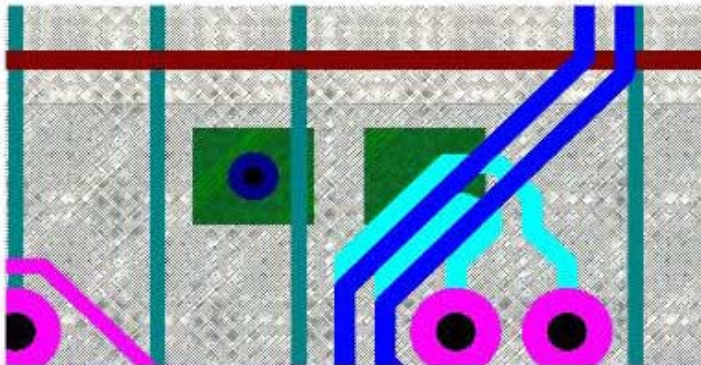
Original Design

- 16 layers
- Through-hole technology
- 1517-pin FPBGA
 - Dominates the board
 - Many 50-ohm signals
 - Many 100-ohm diff pairs
- 940-pin BGA
- 498-pin BGA
- 16 144-pin flash memory
 - Pins at 0.8mm pitch
- 10x7.8 inches
- Full 1.5V power plane, split 1.25V, 2.5V, and 3.3V power plane

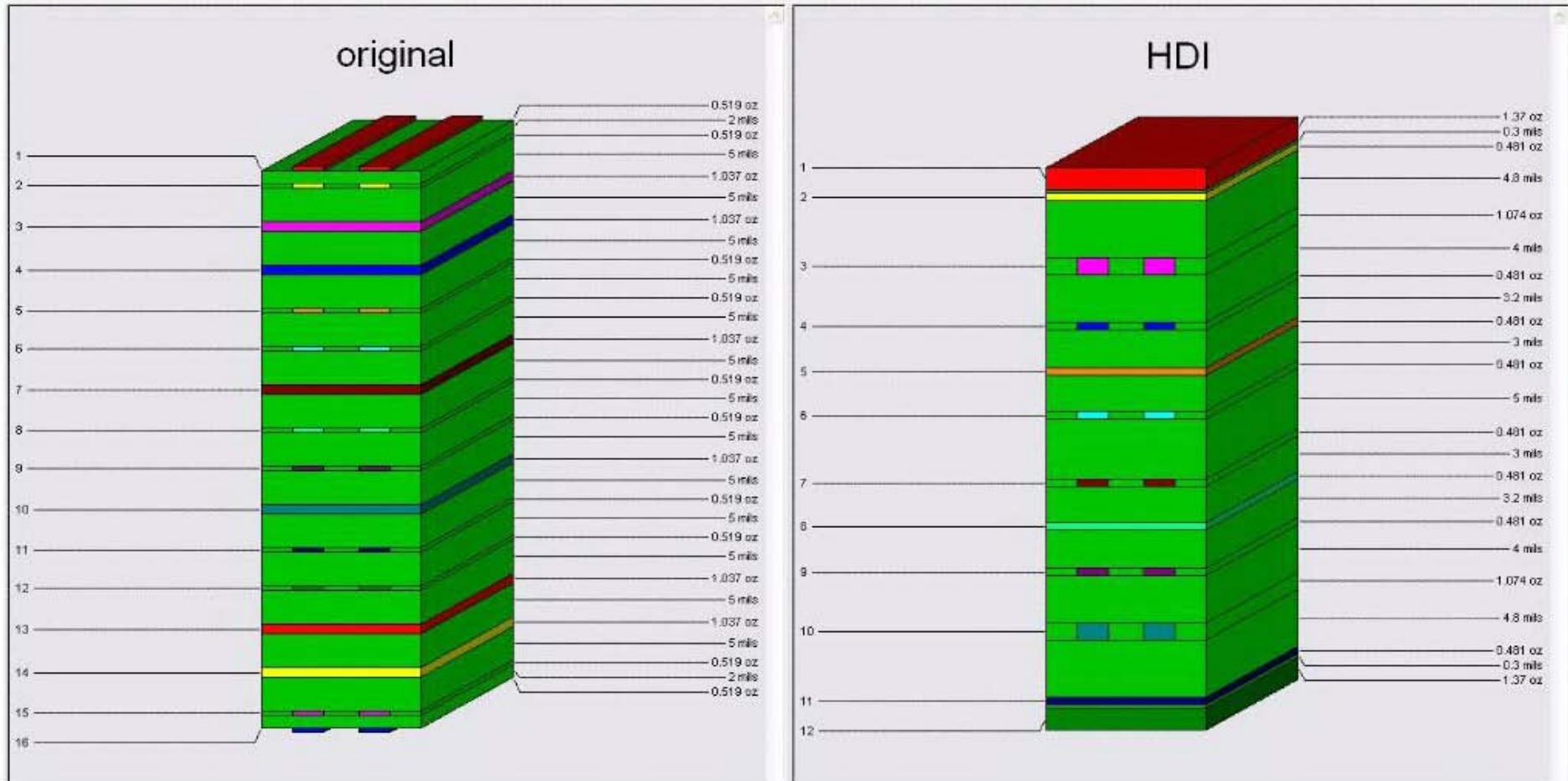


HDI Re-design

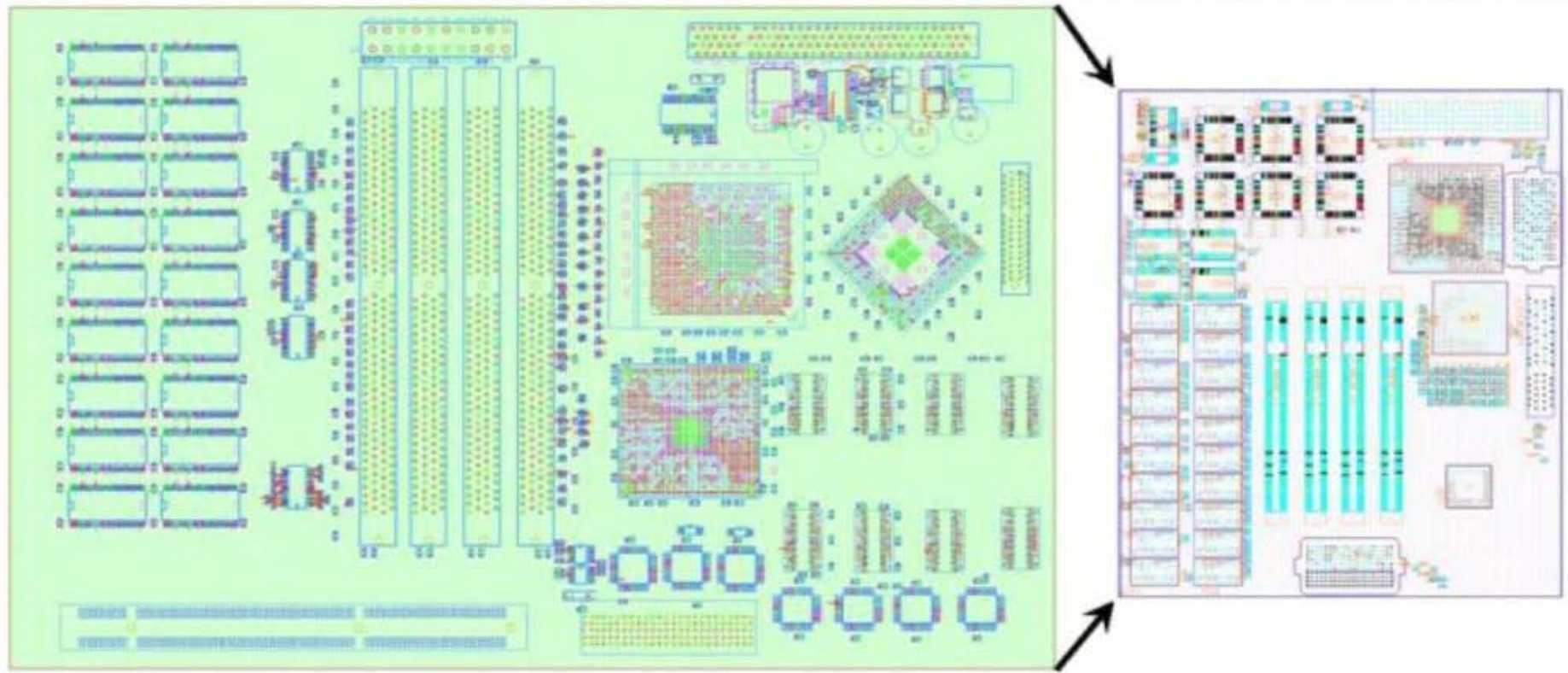
- From 16 to 12 layers
 - Power/ground planes at top and bottom of board
 - C-ply between planes
 - 0.3 mils thick, $E_r = 16$
- From 10"x7.8" to 5"x6"
- Used fine-pitch versions BGAs
 - 0.8mm, 0.65mm, and 0.5mm
- Utilizes via-in-pad technology



Original versus HDI Design



Original versus HDI Design



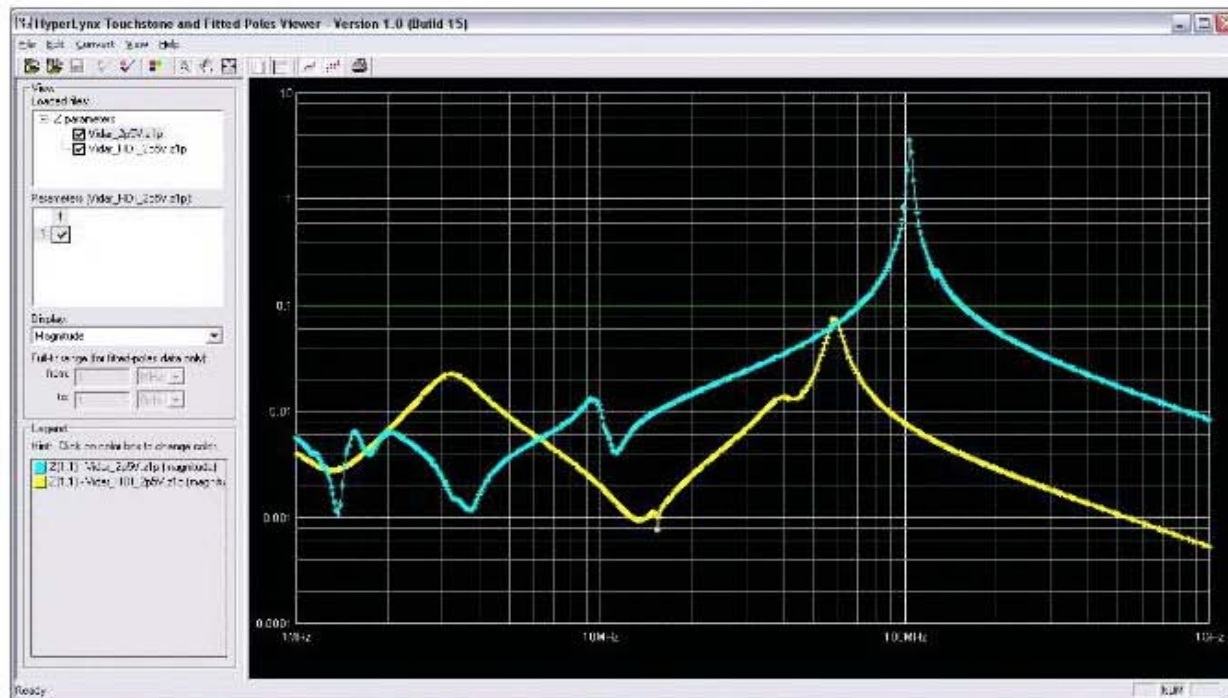
PDN impedance for 2.5V

■ Original design

- 30 0.01uF caps
- 88 0.1uF caps
- 1 10uF cap

■ HDI design

- 4 0.01uF caps
- 42 0.1uF caps
- 1 10uF cap



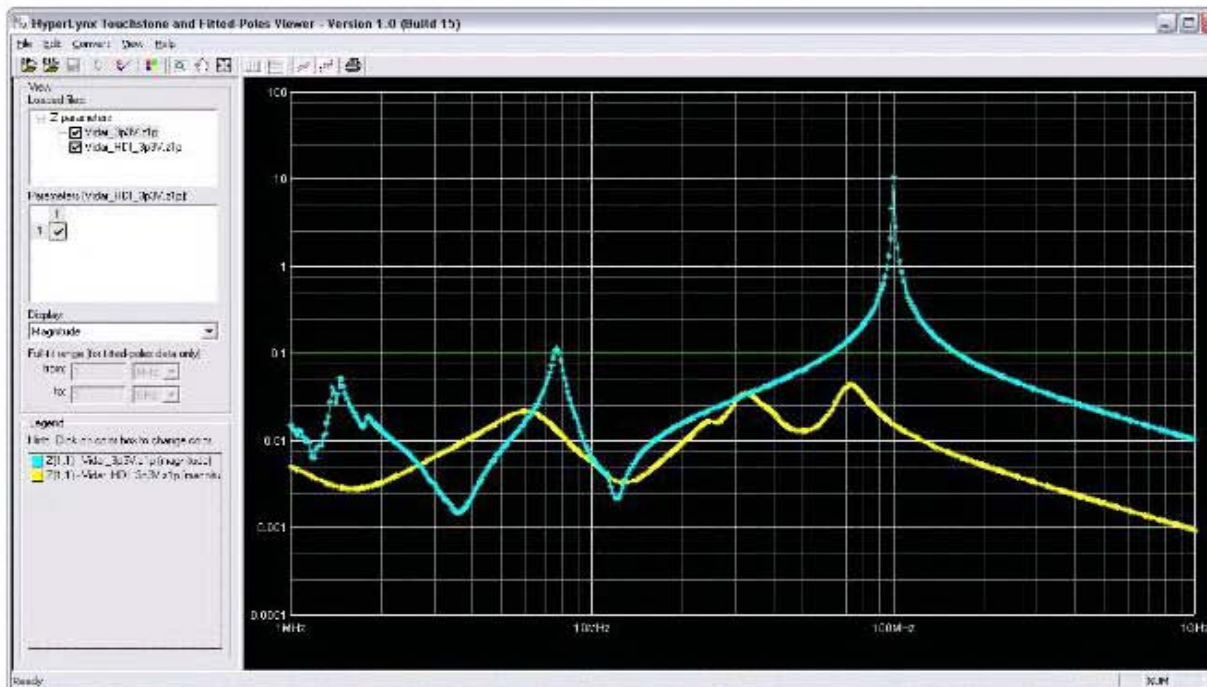
PDN impedance for 3.3V

■ Original design

- 100 0.01uF caps
- 60 0.1uF caps
- 1 1200uF cap

■ HDI design

- 12 0.01uF caps
- 14 0.1uF caps
- 1 1200uF cap



Cost compare

Estimated price matrix HDI

| Layer | PTH | 1+n+1 no burr. | 1+n+1 (cu filled) | 1+nb+1 | 1+nb+1 (cu filled) | 2+(n)+2 stagg. | 2+(n)+2 Stacked | 2+(nb)+2 stagg. | 2+(nb)+2 Stacked |
|-------|-----|-------------------|----------------------|--------|-----------------------|-------------------|--------------------|--------------------|---------------------|
| 6 | 1,0 | 2,3 | 2,5 | 2,9 | 3,2 | 2,7 | 3,0 | 3,4 | 3,7 |
| 8 | 1,4 | 2,7 | 3,0 | 3,4 | 3,6 | 3,6 | 3,9 | 4,3 | 4,6 |
| 10 | 1,8 | 3,3 | 3,6 | 4,0 | 4,2 | 4,1 | 4,4 | 4,8 | 5,1 |
| 12 | 2,3 | 3,8 | 4,1 | 4,5 | 4,8 | 4,7 | 5,1 | 5,4 | 5,8 |
| 14 | 2,8 | 4,6 | 4,8 | 5,2 | 5,5 | N/A | N/A | N/A | N/A |
| 16 | 3,5 | 5,4 | N/A | 6,5 | N/A | N/A | N/A | N/A | N/A |

PCB Data

Track / space 4/4 mil. Drill size min 0.20mm, μ via 0.10mm, Immersion Ag or ENIG, Soldermask wetfilm, Material FR4 TG150, mechanical hole density is max 50/inch², board thickness = or <1.6mm, cu thickness 1oz or 0.5oz impedance control = or < 2, Board Dimensions (Utilization) > or = 80%